LISTING OF THE CLAIMS

Please amend the claims as follows:

1. (Currently Amended) A gate driving apparatus for a liquid crystal display, comprising:

a shift register provided with first and second half-period clock signals having phases inverted with respect to each other, first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period, a start pulse, a high-level supply voltage and a low-level supply voltage,

wherein the shift register generates a half-period output in response to the start pulse and the first and second half-period clock signals, and generates a one-period output at a half-period delay from an end time of the half-period output in response to any one of the first to fourth one-period clock signals, and

wherein each of the first and second half-period clock signals has a pulse width that is half of the pulse width of the first and fourth one-period clock signals.

2. (Original) The gate driving apparatus of claim 1, wherein the shift register includes a plurality of stages for generating the half-period output and the one-period output and further wherein the stages are connected in a cascade arrangement for sequentially shifting the half-period output and the one-period output.

3. (Original) The gate driving apparatus of claim 1, wherein any one of the first and second half-period clock signals, any one of the first to fourth one-period clock signals and the start pulse are synchronized with each other.

4. (Currently Amended) A gate driving apparatus for a liquid crystal display, comprising:

a first input circuit for charging a first charge control node in response to a start pulse and a first half-period clock signal of first and second half-period clock signals having phases inverted with respect to each other and each having a half-period pulse width, and for charging a first discharge control node in response to the first half-period clock signal and a first clock signal of first to third clock signals having phases shifted sequentially and each having a one-period pulse width; and

a first output circuit for outputting a half-period output to an output node in response to a control signal from the first charge control node and the second half-period clock signal, and for discharging the output node in response to a control signal from the first discharge control node,

wherein each of the first and second half-period clock signals has a pulse width that is half of the pulse width of the first and fourth one-period clock signals.

5. (Original) The gate driving apparatus of claim 4, further comprising:

a second input circuit for charging a second charge control node in response to the half-period output and the first half-period clock signal, and for charging the second charge control node in response to the second clock signal; and

a second output circuit for outputting a one-period output to the output node at a half-period delay from an end time of the half-period output in response to a control signal from the second charge control node and the third clock signal, and for discharging the output node in response to a control signal from the second discharge control node.

6. (Original) The gate driving apparatus of claim 5, wherein the first input circuit, the

first output circuit, the second input circuit and the second output circuit are included in each of a plurality of stages.

7. (Original) The gate driving apparatus of claim 6, wherein the start pulse is applied to the first stage of the plurality of stages.

8. (Previously Presented) The gate driving apparatus of claim 4, wherein the first half-period clock signal is synchronized with the second clock signal and the start pulse.

9. (Original) The gate driving apparatus of claim 4, wherein the first input circuit includes an inverter for charging the first charge control node at a half-period delay from the end time of the start pulse in response to the start pulse and the first half-period clock signal.

10. (Previously Presented) The gate driving apparatus of claim 9, wherein the inverter includes:

a first transistor having a gate electrode and a drain electrode supplied with the start pulse;

a second transistor having a gate electrode supplied with the second half-period clock signal and a source electrode supplied with a high-level supply voltage; and

a third transistor having a gate electrode connected to a drain electrode of the first transistor, a source electrode connected to a drain electrode of the second transistor, and a drain electrode connected to the first charge control node.

11. (Original) The gate driving apparatus of claim 10, wherein the inverter further includes a capacitor for charging the start pulse to apply a gate voltage to the gate electrode of

the third transistor.

12. (Previously Presented) The gate driving apparatus of claim 10, wherein the first input circuit includes:

a fourth transistor having a gate electrode supplied with the fourth clock signal, a drain electrode supplied with a low-level supply voltage, and a source electrode connected to the gate electrode of the third transistor; and

a fifth transistor having a drain electrode supplied with the low-level supply voltage, a gate electrode connected to the first discharge control node, and a source electrode connected to the first charge control node.

13. (Previously Presented) The gate driving apparatus of claim 4, wherein the first input circuit includes:

a sixth transistor having a gate electrode supplied with the fourth clock signal and a source electrode supplied with a high-level supply voltage; and

a seventh transistor having a gate electrode supplied with the second half-period clock signal, a source electrode connected to a drain electrode of the sixth transistor, and a drain electrode connected to the first discharge control node.

14. (Original) The gate driving apparatus of claim 4, wherein the first input circuit includes:

an eighth transistor having a gate electrode supplied with the start pulse, a drain electrode supplied with a low-level supply voltage, and a source electrode connected to the first discharge control node; and

a ninth transistor having a drain electrode supplied with a low-level supply voltage, a gate

electrode connected to the output node and a source electrode connected to the first discharge control node.

15. (Previously Presented) The gate driving apparatus of claim 6, wherein the first output circuit includes:

a tenth transistor having a source electrode supplied with the first half-period clock signal, a drain electrode connected to the output node, and a gate electrode connected to the first charge control node;

an eleventh transistor having a drain electrode supplied with a low-level supply voltage, a source electrode connected to the output node, and a gate electrode connected to the first discharge control node; and

a twelfth transistor having a source electrode supplied with the first half-period clock signal, a gate electrode connected to the first charge control node, and a drain electrode connected to a start pulse input terminal of the next stage.

16. (Original) The gate driving apparatus of claim 5, wherein the second input circuit includes an inverter for charging the second charge control node at a half-period delay from the end time of the half-period output in response to the half-period output and the first half-period clock signal.

17. (Previously Presented) The gate driving apparatus of claim 16, wherein the inverter includes:

a thirteenth transistor having a source electrode supplied with a high-level supply voltage and a gate electrode connected to the output node;

a fourteenth transistor having a source electrode supplied with the high-level supply

voltage and a gate electrode supplied with the second half-period clock signal; and

a fifteenth transistor having a gate electrode connected to a source electrode of the thirteenth transistor, a source electrode connected to a drain electrode of the fourteenth transistor, and a drain electrode connected to the second charge control node.

18. (Original) The gate driving apparatus of claim 17, wherein the inverter further includes a capacitor for charging the high-level supply voltage to apply a gate voltage to the gate electrode of the fifteenth transistor.

19. (Previously Presented) The gate driving apparatus of claim 17, wherein the second input circuit includes:

a sixteenth transistor having a gate electrode supplied with the first clock signal, a drain electrode supplied with a low-level supply voltage, and a source electrode connected to the drain electrode of the thirteenth transistor and the gate electrode of the fifteenth transistor; and

a seventeenth transistor having a drain electrode supplied with the low-level supply voltage, a gate electrode connected to the second discharge control node, and a source electrode connected to the drain electrode of the fifteenth transistor and the second charge control node.

20. (Previously Presented) The gate driving apparatus of claim 5, wherein the second input circuit includes:

an eighteenth transistor having a gate electrode and a source electrode supplied with the third clock signal and a drain electrode connected to the second discharge control node;

a nineteenth transistor having a drain electrode supplied with a low-level supply voltage, a gate electrode connected to the output node, and a source electrode connected to the second discharge node; and

a twentieth transistor having a drain electrode supplied with the low-level supply voltage, a gate electrode connected to the second charge control node, and a source electrode connected to the second discharge control node.

21. (Previously Presented) The gate driving apparatus of claim 5, wherein the second output circuit includes:

a twenty-first transistor having a source electrode supplied with the first clock signal, a gate electrode connected to the second charge control node, and a drain electrode connected to the output node; and

a twenty-second transistor having a drain electrode supplied with a low-level supply voltage, a gate electrode connected to the second discharge control node, and a source electrode connected to the output node.

22. (Currently Amended) A gate driving method for a liquid crystal display, comprising the steps of:

receiving first and second half-period clock signals having phases inverted with respect to each other and each having a half-period of pulse width, first to fourth one-period clock signals having phases shifted sequentially and each having a pulse width of one period, a start pulse, a high-level supply voltage and a low-level supply voltage; and

generating a half-period output in response to the start pulse and the first and second half-period clock signals, and generating an one-period output at a half-period delay from the end time of the half-period output in response to any one of the first to fourth one-period clock signals, and

wherein each of the first and second half-period clock signals has a pulse width that is half of the pulse width of the first and fourth one-period clock signals.

23. (Original) The gate driving method of claim 22, wherein any one of the first and second half-period clock signals, any one of the first to fourth one-period clock signals and the start pulse are synchronized with each other.

24. (Currently Amended) A gate driving method for a liquid crystal display, comprising the steps of:

charging a first charge control node in response to a start pulse and a first half-period clock signal of first and second half-period clock signals having phases inverted with respect to each other and each having a half-period pulse width;

outputting an half-period output to an output node in response to a control signal from the first charge control node and the first half-period clock signal;

charging a first discharge control node in response to the second half-period clock signal and a first clock signal of first to third clock signals having phases shifted sequentially and each having an one-period pulse width;

discharging the output node in response to a control signal from the first discharge control node;

charging the second charge control node in response to the half-period output and the second half-period clock signal;

charging the second discharge control node in response to the second clock signal;

outputting a one-period output to the output node at a half-period delay from an end time of the half-period output in response to a control signal from the second charge control node and the third clock signal; and

discharging the output node in response to a control signal from the second discharge control node.

wherein each of the first and second half-period clock signals has a pulse width that is half of the pulse width of the first and fourth one-period clock signals.

25. (Original) The gate driving method of claim 24, wherein the first half-period clock signal, the second clock signal, and the start pulse are synchronized with each other.